REMARKS

Claims 1-7, 11, and 13-21 remain in the application. Claims 1, 6, 11, 13-14, 17, and 20 have been amended. Claims 8-10 and 12 have been cancelled.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached pages are captioned "**Version with marking to show changes made.**"

I. SUMMARY OF THE JULY 31ST, 2002 OFFICE ACTION.

A. Objection

The Office Action requests updating of U.S. Patent application numbers to reflect any change of status under the heading: Cross References to Related Applications and on page 8, last paragraph. This has been carried out.

B. Restriction

The Office Action repeats the original telephone restriction of the claims into two groups:

I. a process for forming an integrated circuit, and

II. a process for forming a dual damascene structure.

Applicants originally elected specie I, with traverse. It remains Applicants' position that other than the name, there is not a patentable distinction between the claims of the two groups. Attention is invited to amended claim 6 which now comprises the limitations of claim 1 (from which claim 6 formerly depended), claim 2 (which depends from claim 1), and claim 12, (which originally depended from claim 6). The product formed by amended claim 6 may be deemed to be a dual damascene structure in the broadest sense, and certainly practice of the process of claim 13, which now depends from amended claim 12, would result in formation of a dual

damascene structure. Attention is also invited to the processes described in claims 14 and 16. Finally, to put the matter to rest, and to avoid further confusion, Applicants have cancelled the words "dual damascene" from each of the two independent claims in the second group. All of the remaining claims (Claims 1-7 and 11-21) may now be grouped together as a process for forming multiple layer structures including at least one layer of low k dielectric material by densifying the surfaces of one or more layers of low k dielectric material.

C. **Section 102 Rejections**

Claims 1-3 and 5 were rejected under 35 U.S.C. § 102(b) as being anticipated by Wang et al. U.S. Patent 6,028,015.

D. **Section 103 Rejections**

Claims 4 and 6-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang et al. U.S. Patent 6,028,015 in view of Yau et al. U.S. Patent 6,054,379.

II. THE REFERENCES

A. **The Wang et al. Reference**

Wang et al. U.S. Patent 6,028,015 describes a process for protecting a low dielectric constant organo silicon oxide insulation layer against absorption of moisture by treating exposed surfaces of the low k material with a hydrogen plasma. When forming openings such as vias or trenches in such low k material, a photoresist mask is conventionally employed and then subsequently removed after formation of the openings. However, when the dielectric material in which the opening is formed comprises a low k material, having organic material bonded to the silicon, subsequent removal of the resist mask by oxidation or ashing processes results in damage to the bonds (severance) between the organic materials and the silicon atoms, resulting in oxidation of the organic material, leaving silicon atoms with dangling bonds. Such dangling

bonds of the damaged silicon atoms are capable of bonding with hydroxyl atoms, resulting in the absorption of undesired moisture on and in the low k insulation material. Wang et al.'s treatment of their low k insulation material with a hydrogen plasma is to repair an already damaged low k material by providing a source of energized hydrogen atoms which can bond with the damaged silicon atoms having the dangling bonds to thereby remove potential sites for moisture absorption.

B. **The Yau et al. Reference**

Yau et al. U.S. Patent 6,054,379 discloses a process for forming a low k composite layer of dielectric material comprising a low k layer of insulating material protected by a low k liner layer beneath the low k layer and a low k capping layer above or over the low k layer. The low k liner and capping layers are formed by reacting an organo silane with an oxidizing agent such as nitrous oxide in a PECVD reaction, while the main low k layer is formed by reacting organo silane with an oxidizing agent such as hydrogen peroxide in a PECVD process. By forming both the liner and capping layers of low k dielectric material, the overall dielectric constant of the composite layer is reduced.

III. THE INVENTION

The invention comprises a process for forming a layered integrated circuit structure having at least one layer of low k dielectric material. The process for making the structure comprises: first forming a layer of low k dielectric material over a substrate such as a previously formed integrated circuit structure; and then (before exposing the layer of low k dielectric material to any etchant treatment) treating the upper surface of the layer of low k dielectric material with a plasma to form (from the surface portion of the layer of low k insulation material) a layer of densified dielectric material which extends over the remainder of the underlying layer of low k dielectric material.

Optionally, a second layer of low k dielectric material may be formed over the just-formed layer of densified dielectric material, after which this second layer of low k dielectric material is treated in the same manner to form a second layer of densified dielectric material over the second layer of low k dielectric material. The layer or layers of densified dielectric material formed from the low k dielectric material provide mechanical support to the remainder of the structure, and can further function as etch stop and mask layers for the formation of vias and/or trenches. The formation of a stack of layers comprising two such densified layers, each over a layer of low k dielectric material, may also be used to form a dual damascene structure.

IV. DISCUSSION

Claims 1-3 and 5 were rejected under 35 U.S.C. § 102(b) as being anticipated by Wang et al. U.S. Patent 6,028,015. Claims 4 and 6-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang et al. U.S. Patent 6,028,015 in view of Yau et al. U.S. Patent 6,054,379.

A. Patentability Over the Wang et al. reference - U.S. Patent 6,028,015

The Wang et al. patent is directed to a process for treating ***already damaged*** low k insulation material with a hydrogen plasma to react with the broken bonds When forming, for example, vias in such low k dielectric material, the low k insulation material is first masked with a photoresist mask, and then etched to form openings in the low k material. The structure is then subject to an oxidation or ashing process which removes the resist mask, but also attacks and severs some of the organic-silicon bonds, oxidizing the organic portion of the bond, and leaving silicon atoms capable of reacting with hydroxyl atoms to form undesirable moisture-containing low k insulation material. The Wang et al. treatment remedies this by providing energized hydrogen atoms to react with such reactive bonds on the damaged silicon atoms ***after*** the steps

of forming a resist mask on the layer of low k insulation material, ***after*** etching openings in the low k material through the mask, and then ***after*** removing the mask.

In contrast, Applicants' process is directed to the densification or alteration of the surface of a low k insulation material with a plasma ***before*** formation of a mask over the low k layer, ***before*** etching of openings in the low k layer though the mask, and ***before*** removal of the etch mask by an oxidation or ashing process. Applicants' purpose in treating such low k material to densify it is to form a different material on the surface of the low k material to thereby provide a material with different responses to etchant materials than the underlying untreated low k material, thus rendering the densified material suitable for use as an etch stop layer or even as a mask itself. Applicants' claimed invention is neither anticipated nor suggested by the teachings of Wang et al.

B. **Patentability Over the Combination of the Wang et al. Reference with the Yau et al. Reference - U.S. Patent 6,054,379**

The Rejection indicates that the deficiencies in the teachings of the principle Wang et al. are made up for by borrowing from the '379 Yau et al. patent. However, these two patents are directed to two entirely different teachings, namely the repair of an etch-damaged region of a low k dielectric material (Wang et al.); and the formation of a main layer of low k dielectric material having a liner of low k material beneath the main layer and another layer of low k dielectric material serving as a capping layer wherein the different layers of low k material are formed by respectively reacting different oxidizing agents with an organo silane.

It is Applicants' position that one would not think to combine the teachings of such widely disparant patents to somehow come up with Applicants' claimed process. A cook in a kitchen, seeking to find a recipe for cooking meat does not combine a recipe for making candy with a recipe for salad, even though all of the above are direct to the formation of a food product. Put another way, to properly combine references together, one must find some

suggestions in the references for the desirability of combining reference together in the manner proposed by the USPTO.

In the case of In re Imperato 179 USPQ 730, the CCPA stated, at page 732:

> "With regard to the principle rejection, we agree that combining the teaching of Schaefer with that of Johnson or Amberg would give the beneficial result observed by appellant. However, the mere fact that these disclosures ***can*** be combined does not make the combination obvious unless the art also contains something to suggest the desirability of the combination." (Emphasis in original text)

The In re Imperato case was cited with approval by the District of Columbia District Court in Berghauser v. Dann, Commissioner of Patents 204 USPQ 393 at page 396.

In the case of In re Regal, Buchel and Plempel, 188 USPQ 136 (1975), the CCPA stated on page 139:

> "...there must be some logical reason, apparent from positive, concrete evidence of record which justifies a combination of primary and secondary references...Further, as we stated in re Bergel...130 USPQ 206, 208 (1961): The mere fact that it is ***possible*** to find two isolated disclosures which might be combined in such a way to produce a new compound does not necessarily render such production obvious unless the art also contains something to suggest the desirability of the proposed combination." (Emphasis in original)

The Court of Appeals for the Federal Circuit (CAFC) has continued to require that there be such a suggestion of desirability of such combinations and/or such modifications in references being cited. (C. Lindemann Maschinenfabrik GmBh v. American Hoist & Derrick, 221 USPQ 481, Fed. Cir., 1984; ACS Hospital Systems, Inc. v. Montefiore Hospital et al, 221 USPQ 929, Fed. Cir., 1984; In re Gordon, 221 USPQ 1125, Fed. Cir., 1984; and In re Grabiak, 226 USPQ 870, Fed. Cir., 1985.)

In Lindemann, the Court stated, at page 488:

> "The claimed invention must be considered as a whole, and the question is whether there is something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination."

The court then cited, with approval, In re Imperato, 179 USPQ 730, and In re Sernaker, 217 USPQ 1.

In the ACS Hospital Systems case, the CAFC stated, at page 933:

> "Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under section 103, teachings of references can be combined ***only*** if there is some suggestion or incentive to do so. The prior art of record fails to provide any such suggestion or incentive." (Emphasis in original)

The ACS Hospital Systems case was later cited with approval in the case of In re Geiger, 2 USPQ 2d 1276, Fed. Cir., 1987, at page 1278.

In the case of In re Gordon, the CAFC stated, at page 1127:

> "The mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification."

In the Case of In re Grabiak, the CAFC, at page 872, repeated the statement in the CCPA case of In re Bergel (130 USPQ 206), that:

> "The mere fact that it is ***possible*** to find two isolated disclosures which might be combined in such a way to produce a new compound does not necessarily render such production obvious unless the art also contains something to suggest the desirability of the proposed combination." (Emphasis in original)

More recently the CAFC stated, in the case of In re Newell, 13 USPQ 2d 1248 (1989), at page 1250:

> "..a retrospective view of inherency is not a substitute for some teaching or suggestion which supports the selection and use of the various elements in the particular claimed combination."

In the case of In re Rouffert, 47 USPQ 2d 1453 Fed. Cir., 1998, the CAFC stated, at page 1456:

> "When a rejection depends on a combination of prior art references, there must be some teaching, suggestion, or motivation to combine the references."

citing with approval In re Geiger, 2 USPQ 2d 1276, Fed. Cir., 1987, at page 1278.

The CAFC has also held that a reference may not be considered in less than its entirety and that disclosures in a reference that diverge from or teach away from the invention, may not be disregarded. In the case of W.L. Gore and Associates v. Garlock, Inc., 220 USPQ 303, the CAFC stated, at page 311:

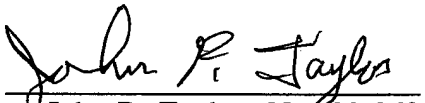
> "In its consideration of the prior art, the district court erred...in considering the references in less than their entireties, i.e., in disregarding disclosures in the references that diverge from and teach away from the invention at hand."

In the case of Bausch & Lomb v. Barnes-Hind/Hydrocurve, 230 USPQ 416, the CAFC reaffirmed its position on using only selected portions of a reference by quoting, on page 419, the following excerpt from an earlier CCPA case (In re Weslau, 147 USPQ 391):

> "It is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position to the exclusion of other parts necessary to a full appreciation of what such reference fairly suggests to one skilled in the art."

It is Applicants' position that the teachings of Wang et al. and Yau et al. cited references, when taken as a whole, do not suggest Applicants' claims. If the Examiner in charge of this case feels that there are any remaining unresolved issues in this case, the Examiner is urged to call the undersigned attorney at the below listed telephone number which is in the Pacific Coast Time Zone.

Respectfully Submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The paragraph beginning at page 1, line 6, has been amended as follows:

The subject matter of this application relates to the subject matter of ~~copending~~ U.S. Patent ~~Application Serial~~ No. 6,350,700, issued February 26, 2002, ~~09/607,512~~ entitled "PROCESS FOR FORMING TRENCHES AND VIAS IN LAYERS OF LOW DIELECTRIC CONSTANT CARBON-DOPED SILICON OXIDE DIELECTRIC MATERIAL OF AN INTEGRATED CIRCUIT STRUCTURE WHILE INHIBITING DAMAGE TO THE LAYERS OF LOW DIELECTRIC CONSTANT CARBON-DOPED SILICON OXIDE DIELECTRIC MATERIAL", assigned to the assignee of this application, and the subject matter of which is hereby incorporated herein by reference.

The paragraph beginning at page 1, line 13, has been amended as follows:

The subject matter of this application relates to the subject matter of ~~copending~~ U.S. Patent ~~Application Serial~~ No. 6,368,979, issued April 9, 2002, ~~09/607,511~~ entitled "PROCESS FOR FORMING TRENCHES AND VIAS IN LAYERS OF LOW DIELECTRIC CONSTANT CARBON-DOPED SILICON OXIDE DIELECTRIC MATERIAL OF AN INTEGRATED CIRCUIT STRUCTURE", assigned to the assignee of this application, and the subject matter of which is hereby incorporated herein by reference.

The paragraph beginning at page 8, line 17, has been amended as follows:

The layers of low k dielectric material described herein may comprise carbon-doped silicon oxide dielectric material or any other type of low k dielectric material capable of being treated in a plasma to form, from the surface portion of the low k dielectric layer, a densified layer of dielectric material having characteristics resembling a conventional (non-low k) silicon oxide or silicon carbide dielectric material. Low k dielectric material suitable for use in this invention and capable of being treated to form the desired layer or layers of densified dielectric material can be formed using processes and equipment commercially available from, for example, Novellus, AMAT, Trikon, ASM, Dow Corning, Hitachi, Dow Chemical, Honeywell, Schumacher, and W.L. Gore. Other low k dielectric materials which may be used in the process of the invention include the low k dielectric materials described in U.S. Patent No. 6,303,047, issued October 16, 2001, and U.S. Patent Application Serial Nos. ~~09/274,457;~~ 09/590,310; 09/792,683; 09/792,685; and 09/792,691; all assigned to the assignee of the invention; and the subject matter of each of which is hereby incorporated by reference. The formation of densified dielectric material on the surface of a low k dielectric material is also disclosed in Sukharev et al. U.S. Patent No. 6,114,259, issued September 5, 2000 and assigned to the assignee of this application, and the subject matter of which is hereby incorporated herein by reference.

In the Claims:

Claims 8-10 and 12 have been cancelled.

Claims 1, 6, 11, 13-14, 17, and 20 have been amended as follows:

1. (Amended) A process for forming an integrated circuit structure having at least one layer of low k dielectric material therein and a layer, formed from said ~~a~~ low k dielectric material ~~layer~~, suitable for use as an etch stop and/or an etch mask which comprises:

a) forming a first layer of low k dielectric material over a previously formed integrated circuit structure; and

b) then, prior to any exposure of said first layer of low k dielectric material to etchants, treating the upper surface of said first layer of low k dielectric material with a plasma to form a first layer of densified dielectric material over the remainder of the underlying first layer of low k dielectric material;

whereby said first layer of densified dielectric material is capable of serving as a etch stop and/or an etch mask for subsequent etching of said underlying first layer of low k dielectric material.

6. (Amended) A process for forming an integrated circuit structure having at least one layer of low k material therein and a layer, formed from a low k dielectric layer, suitable for use as an etch stop and/or an etch mask which comprises:

a) forming a first layer of low k dielectric material over a previously formed integrated circuit structure; and

b) treating the upper surface of said first layer of low k dielectric material with a plasma to form a first layer of densified dielectric material over the remainder of the underlying first layer of low k dielectric material whereby said first layer of densified dielectric material is capable of serving as an etch stop and/or an etch mask for etching of said underlying first layer of low k dielectric material;

c) patterning said first layer of densified dielectric material to form a first etch mask layer of densified dielectric material having a pattern of openings therein suitable for use in etching a corresponding pattern of openings in said underlying first layer of low k dielectric material; ~~The process of claim 1 including the further step of~~

d) forming a second layer of low k dielectric material over said first layer of densified dielectric material~~.~~;

e) treating the upper surface of said second layer of low k dielectric material to form a second layer of densified dielectric material over the remainder of said second layer of low k dielectric material;

f) patterning said second layer of densified dielectric material to form a second etch mask layer of densified dielectric material over said second layer of low k dielectric material, said second etch mask layer having a pattern of openings therein suitable for use in etching a corresponding pattern of openings in the underlying second layer of low k dielectric material;

g) etching a pattern of openings in said second layer of low k dielectric material through said pattern of openings in said second etch mask layer;

h) forming a pattern of openings in said first etch mask layer through said pattern of openings formed in said second layer of low k dielectric material; and

i) etching a pattern of openings in said first layer of low k dielectric material through said pattern of openings in said first etch mask layer.

11. (Amended) The process of claim 6 ~~10~~ including the further steps of:

a) forming another etch mask over said second etch mask layer, said another mask having openings larger than the openings in said pattern of openings in said second etch mask layer; and

b) etching said larger openings through:

i) said second etch mask layer of densified dielectric material; and

ii) said second layer of low k dielectric material;

down to said first etch mask layer of densified dielectric material;

whereby said structure will have a pattern of smaller openings formed in said first layer of low k dielectric material and a pattern of larger openings formed in said second layer of low k dielectric material and generally in registry with said pattern of smaller openings.

13. (Amended) The process of claim 6 ~~12~~ including the further steps of:

a) forming another etch mask over said second etch mask layer, said another etch mask having openings larger than the openings in said pattern of openings in said second etch mask layer; and

b) etching said larger openings through:

i) said second etch mask layer; and

ii) said second layer of low k dielectric material;

down to said first etch mask layer, using said another etch mask;

whereby said structure will have a pattern of smaller openings formed in said first layer of low k dielectric material and a pattern of larger openings formed in said second layer of low k dielectric material and generally in registry with said pattern of smaller openings.

14. (Amended) The process of claim 6 ~~12~~ wherein said openings formed in said first and second layers of low k dielectric material and said first and second etch mask layers comprise vias, and said process includes the further steps of:

a) forming a trench mask over said second etch mask layer, said trench mask having openings larger than said vias in said second etch mask layer; and

b) etching said trenches through:

i) said second etch mask layer; and

ii) said second layer of low k dielectric material;

down to said first etch mask layer;

whereby said structure will have a pattern of vias formed in said first layer of low k dielectric material and a pattern of trenches formed in said second layer of low k dielectric material, with said trenches in registry with said vias.

17. (Amended) A process for forming a ~~double damaseene~~ structure having a low k material therein which comprises:

a) forming a first layer of dielectric material over an integrated circuit structure;

b) forming a first layer of low k dielectric material over said first layer of dielectric material;

c) treating the upper surface of said first layer of low k dielectric material to form a first layer of densified dielectric material over the remainder of said first layer of low k dielectric material;

d) forming a second layer of low k dielectric material over said first layer of densified dielectric material;

e) treating the upper surface of said second layer of low k dielectric material to form a second layer of densified dielectric material over the remainder of said second layer of low k dielectric material;

f) forming over said second layer of densified dielectric material a via mask having a pattern of via openings therein;

g) etching via openings in said dielectric layers down to said integrated circuit structure through said via mask;

h) forming a trench mask over said second layer of densified dielectric material, said trench mask having a pattern of trench openings therein in registry with said via openings; and

i) etching trenches in said second layer of densified dielectric material and said second layer of low k dielectric material through said trench mask, stopping at said first layer of densified dielectric material.

20. (Amended) A process for forming a ~~double damascene~~ structure having a low k material therein which comprises:

a) forming a first layer of dielectric material over an integrated circuit structure;

b) forming a first layer of low k dielectric material over said first layer of dielectric material;

c) treating the upper surface of said first layer of low k dielectric material to form a first layer of densified dielectric material over the remainder of said first layer of low k dielectric material;

d) forming over said first layer of densified material a via mask having a pattern of via openings therein;

e) etching said first layer of densified material through said via mask to replicate in said first layer of densified material said pattern of via openings in said via mask;

f) removing said via mask;

g) forming a second layer of low k dielectric material over said first layer of densified dielectric material;

h) treating the upper surface of said second layer of low k dielectric material to form a second layer of densified dielectric material over the remainder of said second layer of low k dielectric material;

i) forming over said second layer of densified dielectric material a trench mask having a pattern of trench openings therein in registry with said pattern of via openings in said first layer of densified material;

j) etching said pattern of trench openings in said second layer of densified dielectric material through said trench mask to replicate in said second layer of densified material said pattern of trenches in said trench mask;

k) then continuing said trench etch through said second layer of low k dielectric material down to said first layer of densified dielectric material, thereby exposing, at the bottom

of said trenches, said pattern of via openings formed in said first layer of densified material; and

l) then etching vias in said first layer of dielectric material and said first layer of low k dielectric material dielectric layers down to said integrated circuit structure through said exposed pattern of openings previously formed in said first layer of densified material at the bottom of said trenches.